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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,847	12/10/2001	Theodore J. Letavic	US 010610	3619

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS  
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EXAMINER  
LEWIS, MONICA

ART UNIT  
2822

PAPER NUMBER

DATE MAILED: 05/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/015,847

Applicant(s)

LETAVIC ET AL.

Examiner

Monica Lewis

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 13 February 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-12 and 21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 and 21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. This action is in response to the amendment filed February 13, 2004.

#### *Response to Arguments*

2. Applicant's arguments with respect to claims 1-12 and 21 have been considered but are moot in view of the new ground(s) of rejection.

#### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 8 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Merchant (U.S. Patent No. 5,412,241).

In regards to claim 1, Merchant discloses the following:

a) a buried oxide layer (2) formed over a semiconductor substrate (3) (For Example: See Figure 1);

b) a silicon layer (1) formed over the buried oxide layer (For Example: See Figure 1);

c) a top oxide layer (6) formed over the silicon layer (For Example: See Figure 1);

d) a first gate oxide (8) formed over the silicon layer adjacent the top oxide layer (For Example: See Figure 1); and

a) a second gate oxide formed over a portion of the first gate oxide. Note that (G2) can be considered the second gate oxide (For Example: See Marked Up Figure 1).

In regards to claim 2, Merchant discloses the following:

a) the silicon layer comprises a source region (10), a body region (9), and a drift region (4) (For Example: See Figure 1).

In regards to claim 3, Merchant discloses the following:

a) the first gate oxide is formed over the drift region, the body region, and the source region (For Example: See Figure 1).

In regards to claim 4, Merchant discloses the following:

a) wherein the second gate oxide is formed over the first gate oxide between the top oxide layer and the body region (For Example: See Figure 1).

In regards to claim 8, Merchant discloses the following:

a) a buried oxide layer formed over a semiconductor substrate (For Example: See Figure 1);

b) a silicon layer formed over the buried oxide layer, wherein the silicon layer comprises a source region, a body region, and a drift region (For Example: See Figure 1);

c) a top oxide layer formed over the silicon layer (For Example: See Figure 1);

d) a first gate oxide formed over the silicon layer adjacent the top oxide layer (For Example: See Figure 1); and

e) a second gate oxide formed over a portion of the first gate oxide between the top oxide layer and the body region (For Example: See Figure 1).

In regards to claim 21, Merchant discloses the following:

a) a buried oxide layer formed over a semiconductor substrate (For Example: See Figure 1);

b) a silicon layer formed over the buried oxide layer, wherein the silicon layer comprises a source region, a body region, and a drift region (For Example: See Figure 1);

c) a top oxide layer formed over the silicon layer (For Example: See Figure 1);

d) a first gate oxide formed over the silicon layer adjacent the top oxide layer (For Example: See Figure 1); and

e) a second gate oxide formed over a portion of the first gate oxide between the top oxide layer and the body region, wherein the second gate oxide and the first gate oxide form a stepped oxide region (For Example: See Figure 1).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 5 and 9 are rejected under 35 U.S.C. 103(a) as obvious over Merchant (U.S. Patent No. 5,412,241) in view of Letavic et al. (U.S. Patent No. 6,310,378).

In regards to claims 5 and 9, Merchant discloses the following:

a) a field plate (7) formed over the top oxide layer, the first gate oxide (For Example: See Figure 1).

In regards to claims 5 and 9, Merchant fails to disclose the following:

a) a field plate formed over a second gate oxide.

However, Letavic et al. ("Letavic") discloses a field plate formed over a second gate oxide (For Example: See Figure 4). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Merchant to include a field plate formed over a second gate oxide as disclosed in Letavic because it aids in maintaining the desirable breakdown voltage properties (For Example: See Column 2 Lines 49-53).

Additionally, since Merchant and Letavic are both from the same field of endeavor, the purpose disclosed by Letavic would have been recognized in the pertinent art of Merchant.

Art Unit: 2822

7. Claims 6 and 10 are rejected under 35 U.S.C. 103(a) as obvious over Merchant (U.S. Patent No. 5,412,241) in view of Seeds et al. (U.S. Patent No. 3,936,858).

In regards to claims 6 and 10, Merchant discloses the following:

a) the first gate oxide has a thickness in a range of approximately 300-600A (For Example: See Column 2 Lines 39 and 40).

In regards to claims 6 and 10, Merchant fails to disclose the following:

a) a second gate oxide has a thickness in a range of approximately 900-1200A.

However, Seeds et al. ("Seeds") discloses a gate oxide that has a thickness around 1200A (For Example: See Column 8 Lines 52-55). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Merchant to include a gate oxide that has a thickness around 1200A as disclosed in Seeds because it aids in increasing the threshold voltage (For Example: See Column 8 Lines 52-55).

Additionally, the applicant has not established the critical nature of the dimension where the first gate oxide has a thickness in a range of approximately 300-600A, and wherein the second gate oxide has a thickness in a range of approximately 900-1200A. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990).

Finally, since Merchant and Seeds are both from the same field of endeavor, the purpose disclosed by Seeds would have been recognized in the pertinent art of Merchant.

Art Unit: 2822

8. Claims 7 and 11 are rejected under 35 U.S.C. 103(a) as obvious over Merchant (U.S. Patent No. 5,412,241).

In regards to claims 7 and 11, Merchant fails to disclose the following:

a) the first gate oxide has a length of approximately 3-4 $\mu$ m, and wherein the second gate oxide has a length of approximately 1-2 $\mu$ m.

However, the applicant has not established the critical nature of the dimension where the first gate oxide has a length of approximately 3-4 $\mu$ m, and wherein the second gate oxide has a length of approximately 1-2 $\mu$ m. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

9. Claim 12 is rejected under 35 U.S.C. 103(a) as obvious over Merchant (U.S. Patent No. 5,412,241) in view of Seeds et al. (U.S. Patent No. 3,936,858) and Shirahata et al. (U.S. Publication No. 2002/0175380).

In regards to claim 12, Merchant fails to disclose the following:

a) a thickness of approximately 1200A of the second gate oxide results in an increase from approximately  $1e^{12} \text{ cm}^{-2}$  to approximately  $2e^{12} \text{ cm}^{-2}$  of a maximum allowable charge, and a decrease of approximately 30% for a specific-on-resistance of the device.

However, Seeds et al. ("Seeds") discloses a gate oxide that has a thickness around 1200A (For Example: See Column 8 Lines 52-55). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Merchant to include a gate oxide that has a thickness in a range of approximately around 1200A.

Art Unit: 2822

as disclosed in Seeds because it aids in increasing the threshold voltage (For Example: See Column 8 Lines 52-55).

However, Shirahata et al. ("Shirahata") discloses a gate oxide that has various charges (For Example: See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Merchant to include a gate oxide that has a various charges as disclosed in Shirahata because it aids in increasing the threshold voltage.

Additionally, the applicant has not established the critical nature of the dimension where the first gate oxide has a thickness in a range of approximately 300-600A, and wherein the second gate oxide has a thickness in a range of approximately 900-1200A. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

Finally, since Merchant, Seeds and Shirahata are both from the same field of endeavor, the purpose disclosed by Seeds and Shirahata would have been recognized in the pertinent art of Merchant.



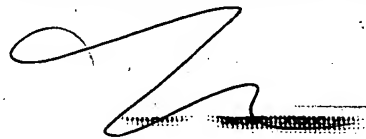
***Conclusion***

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

May 5, 2004



**Mary Wilczewski**  
**Primary Examiner**